REMARKS

This communication is a full and timely response to the aforementioned non-final Office Action dated March 21, 2008. By this communication, claim 2 is canceled without prejudice or disclaimer to the underlying subject matter, and claims 1, 3, and 4 are amended. Claims 1 and 3-10 remain pending, where claims 5-12 are withdrawn. Reconsideration and allowance of this application are respectfully requested.

Rejections Under 35 U.S.C. § 103

Beginning on page 2 of the Office Action, Applicants claims were variously rejected under 35 U.S.C. §103. Namely, claim 1 was rejected under 35 U.S.C. §103(a) for alleged unpatentability over *Vallet et al* (U.S. Patent No. 7,142,621) in view of *Gossmann et al* (U.S. Patent No. 6,359,950); claims 2 and 3 were rejected under 35 U.S.C. §103(a) for alleged unpatentability over *Vallet* in view of *Gossmann* and *Chen et al* (U.S. Patent No. 7,162,002); and claim 4 was rejected under 35 U.S.C. §103(a) for alleged unpatentability over *Vallet* in view of *Gossmann*, *Chen*, and *Ishihara et al* (U.S. Patent No. 5,557,648). Applicants respectfully traverse these rejections.

Claim 1 recites a clock data recovery circuit, comprising in part, a variable delaying unit that generates a delay clock, which is obtained by delaying the clock generated by the voltage control oscillator based on a duty ratio of the input data.

Applicants respectfully submit that the combination of *Vallet*, *Gossmann*, *Chen*, and *Ishihara* fails to establish a *prima facie* case of obviousness in regard to Applicants' claims.

The PTO alleges that *Vallet*, *Gossmann*, and *Chen* discloses the combination of features recited in claim 1 except for a variable delaying unit that delays the clock generated by the voltage control oscillator based on a duty ratio of the input data. The PTO relies on *Ishihara* in an effort to remedy this deficiency.

Ishihara is directed to a phase lock loop circuit having a sample and hold switch circuit that enables a phase locked state to be maintained for a consecutive identical bit state of input data including several tens of consecutive bits. The sample and hold switch circuit is maintained at an off state during the consecutive identical bit state to hold the output of the low-pass filter, so that the voltage controlled oscillator (VCO) continues that frequency at the beginning of the consecutive identical bit state. *See* Abstract. The PTO alleges that the foregoing disclosure describes the use of a duty ratio of input data to control the operation of the VCO. However, upon careful review, Applicants could find no teaching or disclosure that one of ordinary skill would find reasonably related to a duty ratio of the input data as recited in Applicants' claims.

One of ordinary skill would understand that for a series of pulses the duty ratio is defined by the pulse duration divided by the pulse period. As noted above, *Ishihara* discloses that the sample and hold switch circuit is maintained at an off state during the consecutive identical bit state to hold the output of the low-pass filter, so that the voltage controlled oscillator continues that frequency at the beginning of the consecutive identical bit state. The PTO has failed to articulate how one of ordinary skill would interpret or recognize this technique of maintaining a phase locked state could be combined with *Vallet*, *Gossmann*, and *Chen* to achieve Applicants' claimed variable delaying unit that delays the clock generated by the

voltage control oscillator based on a duty ratio of the input data. Thus, it does not appear that one of ordinary skill would have a reasonable or rational basis to look to *Ishihara* or combine this reference with *Vallet*, *Gossmann*, and *Chen* to render Applicants' claims obvious.

In summary, *Vallet*, *Gossmann*, *Chen*, and *Ishihara* when applied individually or collectively fail to discloses every element recited in Applicants' claims and thereby fail to establish a *prima facie* case of obviousness. The PTO is reminded that it has the initial burden of establishing a **factual basis** to support the legal conclusion of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). For rejections under 35 U.S.C. § 103(a) based upon a combination of prior art elements, in *KSR Int'l v. Teleflex Inc.*, 127 S.Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007), the Supreme Court stated that "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some **articulated reasoning with some rational underpinning** to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) (emphasis added). Therefore, withdrawal of this rejection is respectfully requested.

Conclusion

Based on at least the foregoing amendments and remarks, Applicants submit that claims 1, 3, and 4 are allowable. In the event any issues remain, the Office is invited to contact the undersigned attorney.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date: July 21, 2008

By: 
Shawn B. Cage
Registration No. 51522

P.O. Box 1404
Alexandria, VA 22313-1404
703 836 6620